REMARKS

Reconsideration and reexamination of this application in light of the above-amendments and the following remarks is respectfully requested. Claims 1-4, 7-8, 11-16, 19-20, 22-25, and 27-28 are pending in this application. By way of this response Claim 1 has been amended. Support for the amendment can be found throughout the specification and drawings as filed. No new matter has been added. Reconsideration of the rejections set forth in the outstanding Office Action is respectfully requested in view of the following remarks.

I. Objection To The Drawings

The drawings stand objected to under 37 C.F.R. §1.83(a) for not showing every feature of the invention specified in the claims. Applicant requests approval of an amendment of Figure 1 to show a circuit board. Support for showing the circuit board can be found throughout the specification with specific reference to paragraph 18 and Claims 11 and 20. A copy of the redlined Figure 1 as well as a copy of the substitute Figure 1 are included herewith. No new matter has been added. In view of the foregoing, Applicant respectfully requests withdrawal of the objection to the drawings.

II. Rejection Under 35 U.S.C. §112, Second Paragraph

Claims 3, 15, and 24 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicant regards as the invention. Applicant traverses the §112 rejection.

Claim 3 encompasses an integrated chip package in which the heat sink is substantially thermally isolated from the package substrate. The invention of Claim 3 is not limited to including everything that is shown in Figures 1 or 4. For example, the invention of Claim 3 is not limited to including a heat sink that is thermally connected to the package substrate. Instead, as is explicitly recited in Claim 3, the heat sink is substantially thermally isolated from the package substrate.

Similarly, Claims 15 and 24 each include the limitation "further including thermally isolating the heat sink from the package substrate." Claims 15 and 24 are not limited to including every limitation shown in Figures 1 and 4.

III. Rejection Under 35 U.S.C. §103(a)

Claims 1-4, 7-8, 11, 13-16, 19-20, 22-25, 27, and 28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over

Degani et al. (6,282,100B1) in view of Kobayashi et al. Applicant respectfully traverses the rejection.

Claims 1-4, 7-8, 11, 22-25, 27, and 28 are directed to aspects of an integrated chip package and Claims 13-16 and 19-20 are directed to a method of forming an integrated chip package.

Applicant respectfully submits that the combination of Degani with Kobayashi to render Claims 1-4, 7-8, 11, 13-16, 19-20, 22-25, 27, and 28 obvious is a result of hindsight and that the references lack any teaching, suggestion or motivation to combine. Moreover, Applicant asserts that Degani teaches away from making the combination.

"When a rejection depends on a combination of prior art references, there must be some teaching, suggestion, or motivation to combine the references." In re Rouffet, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998). "Close adherence to this methodology is especially important in the case of less technologically complex inventions, where the very ease with which the invention can be understood may prompt one to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." In re Dembeczak, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999). Reliance on "common knowledge and common sense" do not fulfill the Examiner's obligation to cite references to support

an obviousness conclusion. See In re Lee, 61 USPQ2d 1430 (Fed. Cir. 2002). Instead, "particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." In re Kotzab, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). In addition, "references that teach away cannot serve to create a prima facie case of obviousness." In re Gurley, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994). "A prior art reference may be considered to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." Id. page 1131. "If references taken in combination would produce a seemingly inoperative device, … such references teach away from the combination and thus cannot serve as predicates for a prima facie case of obviousness." McGinley v. Franklin Sports, Inc., 60 USPQ2d 1001, 1009 (Fed. Cir. 2001).

The subject matter encompassed by Applicant's Claims 1-4, 7-8, 11, 13-16, 19-20, 22-25, 27, and 28 includes an integrated chip (IC) package in which a heat sink is coupled to a second surface of a semiconductor chip. Here, the heat substantially flows away from the package substrate towards the heat sink. This is supported throughout the specification including

paragraph 13 ("the thermal path of the integrated chip package 10 extends away from the circuit board") and paragraph 16 ("the thermal path of the integrated chip package 10 extends toward the heat sink").

In contradistinction, Degani teaches away from decreasing the heat flowing towards a PCB by extracting heat from the opposite surface of the flip chip IC. Degani does not suggest coupling a heat sink to the flip chip surface that faces away from an intermediate substrate for extracting heat from the flip chip. Instead, Degani teaches using semiconductor as the material for the intermediate substrate (IIS) so that the intermediate substrate is "sufficiently conductive to serve as the bottom conductor level." (col. 4, lines 30-32). Here, Degani teaches using low conductivity material to improve the thermal path from the IC chip 11 towards the printed wiring board 21. Reducing the thermal resistance in the direction of the printed wiring board 21, increases the flow of heat from the IC chip 11 towards the system printed wiring board 28.

In addition, Kobayashi shows attaching a cap (heat sink) 38 to an IC chip 22 that has connection terminals in the form of bumps 24 on the opposing side of the IC chip 22. The bumps 24 connect to a multi-layer substrate 28 (Figures 2-20). The multi-layer substrate 28 does not include attached bonding

wires. Kobayashi does not disclose in any of the 20 figures nor the remainder of the specification attaching a heat sink to a flip chip assembly in which bonding wires are used for interconnection. Instead, in every one of Figures 2-20, the only connections shown are rigid terminals that extend away from the cap 38.

Also, there is no teaching, suggestion or motivation to combine Kobayashi with Degani. Degani is directed to packages with high density interconnections (col. 1, lines 4-5). Degani does not teach or suggest increasing the power handling capability of the package by attaching a heat sink to an opposite surface of the flip chip. Instead, for handling larger ICs, Degani teaches increasing the size of the IIS (col. 4, lines 37-47).

In view of the foregoing, Applicant respectfully submits that Degani combined with Kobayashi is an improper combination and that Claims 1-4, 7-8, 11, 13-16, 19-20, 22-25, 27, and 28 encompass patentable subject matter.

Claims 1-4, 7-8, 11, 13-16, 19-20, 22-25, 27, and 28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Boyle in view of Kobayashi et al. Applicant respectfully traverses the rejection.

Boyle, similar to Degani, teaches away from using a heat sink to increase the power handling capability of an IC module. Boyle teaches an IC module that is suitable for use in ultrahigh vacuum and high temperature environments (col. 4, line 66 to col. 5, line 1). The IC module may include a Charge Coupled Device (CCD) that is configured for backside illumination (col. 5, lines 11-13). Each of the embodiments of the IC module are described and shown as including a CCD (110, 210, 310, 410, 510) configured for backside illumination (see Figures 1-5). For the CCD to receive illumination, the backside of the CCD cannot be covered. Attaching a heatsink to the backside of the CCD would prevent illumination of the CCD and therefore make the IC module inoperative. A combination of references which produce a seemingly inoperative device have been held to teach away from the combination and therefore cannot serve as predicates for a prima facie case of obviousness. McGinley v. Franklin Sports, Inc., 60 USPQ2d 1001, 1009 (Fed. Cir. 2001). Therefore, the combination of Boyle and Kobayashi cannot serve as predicates for a prima facie case of obviousness since attaching a heatsink to the backside of the CCD would make the IC module inoperative.

In addition, Boyle does not teach decreasing the heat flowing towards a PCB by extracting heat from the opposite surface of the flip chip IC. Boyle does not address how to

improve the power handling capability of an IC module. Instead, Boyle teaches an IC assembly in which the fragility of the IC die is a major concern. The IC assembly of Boyle "must be backside thinned to approximately 10 to 20 microns (col. 5, lines 13-14) resulting in a fragile die. To minimize stresses on the thinned die the coefficient of thermal expansion of the carrier is matched to the IC to reduce stresses caused by expansion and contraction of the assembly (col. 5, line 64 to col. 6, line 2). Boyle teaches a system in which the problems addressed and the solutions are entirely different than that described by Applicant's IC package. In fact, Boyle teaches away from decreasing the flow of heat towards the header and instead teaches increasing the flow of heat towards the header by matching the coefficients of thermal expansion of the thinned, fragile die and the carrier. Therefore, Applicant respectfully submits that Boyle combined with Kobayashi is an improper combination and that Claims 1-4, 7-8, 11, 13-16, 19-20, 22-25, 27, and 28 encompass patentable subject matter.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of this rejection of independent claims 1, 13, and 22 as well as dependent claims 2-4, 7-8, 11, 14-16, 19-20, 23-25, 27, and 28 under 35 U.S.C. §103(a).

IV. Conclusion

Applicant submits that the specification and drawings are in order and that all of the claims are now in condition for allowance. Such action is respectfully requested. Applicant(s) petition for a one month extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d). Please apply any other charges or credits to Deposit Account No. 50-1236. If the Examiner would like to discuss the matter further, the undersigned may be contacted at (408) 222-2500.

Attached is a marked-up version of the changes being made by the current amendment.

Respectfully submitted,

Date: 11/6/01

Eric B. Janofsky
Attorney for Applicant
Reg. No. 30,759

Please address all correspondence to:
Eric B. Janofsky
General Patent Counsel
Marvell Semiconductor, Inc.
700 First Avenue, Mail Stop 509
Sunnyvale, CA 94089
General Telephone Number (408) 222-2500
Facsimile (408) 752-9034
Email: sforno@marvell.com
Customer No. 23624

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 1, 13, and 22 have been amended as follows:

1. (Amended) An integrated chip package, comprising:

at least one semiconductor chip having a first surface and a second surface;

an intermediate substrate electrically coupled via conductive bumps to the first surface of the at least one semiconductor chip;

a package substrate having a first surface electrically coupled to the intermediate substrate via a plurality of bonding wires; and

a heat sink thermally coupled to the second surface of the semiconductor chip so that heat generated from the at least one semiconductor chip flows towards the heat sink.

13. (Amended) A method of forming an integrated chip package, comprising:

providing a semiconductor chip having a conductor pattern on a first surface;

electrically coupling the conductor pattern on the semiconductor chip to an intermediate substrate via a first set of conductive bumps;

thermally coupling a second side of the semiconductor chip to a heat sink so that heat generated from the semiconductor chip flows towards the heat sink; and

electrically coupling the intermediate substrate to a first surface of a package substrate via a plurality of bond wires.

22. (Amended) An integrated chip package, comprising:

at least one semiconductor chip configured for flip chip mounting, having a first surface and a second surface;

a package substrate having a first surface and a second surface, the package substrate second surface to electrically couple the integrated chip package to a circuit board via conductive bumps;

a flip chip conversion means electrically coupled between the at least one semiconductor chip first surface and the package substrate first surface; and

a means for sinking heat from the second surface of the semiconductor chip so that heat generated from the semiconductor chip flows towards the means for sinking heat.